REMARKS

At paragraphs 2-4 of the office action, the examiner objects to the drawings. In paragraph 3 the examiner objects because the drawings do not include the references 5A and 5B. In paragraph 4, the examiner objects because there are two sets of figures 5 and 6, pages 6 and 9.

Formal drawings are submitted herewith. Pages 2, 4, 12-14 and 27-28 are amended to make the specification correspond with the drawings. Pages 6 and 9 of the informal drawings are duplicates, both including Figures 5 and 6. The specification has been amended to change Figure 5A to Figure 5, and Figure 5B to Figure 6 to correspond to the formal drawings, and the previous reference to Figure 6 has been deleted to correspond to the informal drawings as filed.

It is respectfully submitted that the formal drawings are allowable, with allowance is respectfully requested.

At paragraph 5 the examiner has requested applicant's cooperation in correcting any errors of which the applicants may become aware. Pages 12-14 and 27-28 are amended to make the specification consistent with the drawings.

At paragraph 6, the examiner objects to page 6, lines 13-16. The reference numbers 160, 155, 180 and 190 are added as requested.

At paragraph 7, the page 2, line 13-21 are objected to because the co-pending applications are not identified by serial numbers. Page 2, lines 13-21 of the application has been amended to include the serial numbers of the copending applications.

It is respectfully submitted that the Specification as amended is allowable, which allowance is respectfully requested.

At paragraphs 8-16, rejections are made under 35 U.S.C. § 112.

At paragraph 9, claims 3 and 16 are rejected wherein the examiner states a "Self-Timed Interface or an STI bus' is not clearly defined in the disclosure or claims. This rejection is respectfully traversed, and reconsideration is requested. The use of a Self-Timed Interface or an STI bus is clearly set out at page 7, line 29 of the specification. A self-timed interface (STI) bus or link is clearly understood by those skilled in the art as evidenced by the U.S. Patent No. 5,598,442 issued to Gregg et al. Jan. 28, 1997 for SELF-TIMED PARALLEL INTER-SYSTEM DATA COMMUNICATION CHANNEL, a copy of which is enclosed for the examiners use.

Claim 7 has been amended changing "said plurality of networks" to --said plurality of network elements-- to provide sufficient antecedent basis, as pointed out by the examiner at paragraph 10.

Claims 9, 18 and 22 have been amended changing "said Connector" to --said Connector Interface Element-- to provide sufficient antecedent basis, as pointed out by the examiner at paragraph 11.

Claims 8, 18 and 22 have been amended changing "said Network Interface Elements" to --said Network Interface Element-- to provide sufficient antecedent basis, as pointed out by the examiner at paragraph 12.

Claims 10 and 19 have been amended changing "an I/O device adapters" to --an I/O device adapter-- to make the meaning clear to overcome the rejection of paragraph 13.

Claim 12 has been amended to claim --wherein said Interface Element performs computing network functions establishing network communications between said application server(s) and said application user(s)-- to overcome the rejection of paragraph 14.

Claim 13 has been amended to claim --wherein said Interface Element performs control unit function-- to overcome the rejection of paragraph 15.

Claim 12 has been amended to change "computing network environment" to claim --computing network functions establishing network communications between said application server(s) and said application user(s)-- to overcome the rejection of paragraph 16.

Further, claim 7 has been amended to change "a web-server" to --a web-server-- to make the meaning of claim 7 clear.

It is respectfully submitted that none of these so far mentioned amendments have been made in response to prior art, and that these amendments make the amended claims allowable under 35 U.S.C. § 112, which allowance is respectfully requested.

At paragraphs 17-31, claims 1-2, 4, 6, 10-13, 14-15, 17, and 19-20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Caldarale et al. (hereinafter Caldarale) USP 6,659,794.

Caldarale discloses a network input/output system for sending and receiving messages between a large scale computer system and

environment (Application Server). Only one input, output and control (UPICT) queue is defined. The Network Interface Controller is totally dedicated to the single Operating System environment. Caldarale describes the ability to control multiple I/O devices through the same interface. Caldarale discloses multiple Network Interface Controllers (NIC) in a single Application Server (see Col. 7, line 35).

Claims 1 and 14 have been amended to make clear that the claimed apparatus establishes processing communication with more than one application server. An interrogator is claimed for examining multiple queues in the queue mechanism to transfer appropriate requests, responses and data between multiple application servers and an application user, thus having the ability to manage queues from multiple different Applications Servers, not just a single Application Server as in Caldarale. This ability is fully explained at page 16, lines 11-21 of the specification.

It is respectfully submitted that claims 1, 14 and the claims depended therefrom are allowable under 35 U.S.C. § 102(b) over Caldarale, which allowance is respectfully requested.

At paragraphs 32, 33, claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Caldarale in view of Carbillet (hereinafter Carbillet) USP 6,256,696.

Carbillet discloses a data processing system wherein the processor of a specific module may directly access the peripherals of another module via the inter-module bus and the other's module local bus. There is no teaching or suggestion that multiple processors may be used with multiple queues in storage for transferring requests, responses and data between

peripherals of another module via the inter-module bus and the other's module local bus. There is no teaching or suggestion that multiple processors may be used with multiple queues in storage for transferring requests, responses and data between multiple application servers of the multiple processors and an application user.

It is respectfully submitted that neither Caldarale nor Carbillet, either alone or in combination teach or suggest a system having a plurality of processors wherein incoming and outgoing data is stored in a main storage in processing communication with more than one application server, including an interrogator which operates independent of the application servers and which examines multiple queues in the main storage to transfer requests, responses and data between application servers and an application user, as claimed in claim 5, depended from claims 4 and 1. It is respectfully submitted that claim 5 is allowable under 35 U.S.C. § 103(a) over Caldarale in view of Carbillet, which allowance is respectfully requested.

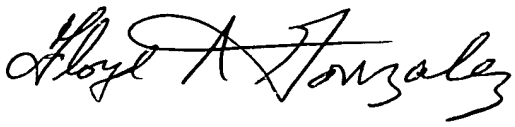
At paragraphs 32 and 34, claims 7 and 8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cladarale in view of Brant et al. (hereinafter Brant) USP 6,081,834. It is respectfully submitted that Cladarale in combination with Brant does not teach or suggest a TCP/IP oriented server in communication with main storage having a queuing mechanism wherein data may be exchanged with more than one application server, as claimed in claims 7 and 8. It is respectfully submitted that claims 7 and 8 are allowable under 35 U.S.C. § 103(a), over Cladarale in view of Brant et al., which allowance is respectfully requested.

At paragraphs 32 and 35, claims 3 and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cladarale in view of Casper et al. (hereinafter Casper) USP 6,192,482. Casper discloses that at the time the present application was filed, a self-timed interface (STI) and STI links were well known by those skilled in the art. There is no teaching or suggestion in Casper that the STI link may be used in connection with main storage having queuing mechanism wherein data may be exchanged with more than one application server, as claimed in claims 3 and 16. It is respectfully submitted that claims 3 and 16 are allowable under 35 U.S.C. § 103(a) over Cladarale in view of Casper, which allowance is respectfully requested.

At paragraphs 32 and 36-39, claims 9, 18, 21 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cladarale in view of Leger et al. (hereinafter Leger) USP 5,765,023. Lager discloses a method and arrangement for performing direct memory access in a computer system having multi-channel direct memory access provided with a host computer having a main memory and a processor that runs software. It is respectfully submitted that neither Lager nor Caldarale teach or suggest a main memory having a queuing mechanism wherein data may be exchanged with more than one application server, as claimed in claims 9, 18, 21 or 22. It is respectfully submitted that claims 9, 18, 21 and 22 are allowable under 35 U.S.C. § 103(a) over Cladarale in view of Leger, which allowance is respectfully requested.

It is respectfully submitted that the present application, as amended herein, is now in condition for allowance, which allowance is respectfully requested.

RESPECTFULLY SUBMITTED



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VERSION WITH MARKINGS TO SHOW CHANGES MADE TO THE SPECIFICATION

The replacement paragraph at page 2, lines 16-21:

This application is [being filed on the same day as the] related to the following [related] copending applications: PO9-99-013, Serial Number 09/253,246; PO9-99-015, Serial Number 09/253,247; PO9-99-016, Serial Number 09/253,248; PO9-99-017, Serial Number 09/252,712; PO9-99-018, Serial Number 09/252,552; PO9-99-019, Serial Number 09/252,728; PO9-99-020, Serial Number 09/252,730; PO9-99-021, Serial Number 09/253,101; PO9-99-022, Serial Number 09/253,286; PO9-99-023, Serial Number 09/252,542; PO9-99-024, Serial Number 09/253,249; PO9-99-025, Serial Number 09/252,556; PO9-99-026, Serial Number 09/253,993; PO9-99-027, Serial Number 09/253,658; PO9-99-028, Serial Number 09/252,555; PO9-99-029, Serial Number 09/255,641; PO9-99-030, Serial Number 09/255,640; and PO9-99-031, Serial Number 09/252,727.

The two replacement paragraphs at page 4, line 1-6:

Figure 5[A] represents the format for the command request block for store-subchannel-QDIO data[, while];

Figure [5B] 6 represents the format for the command response block for the store-subchannel-QDIO data command;

[Figure 6 is an illustration of the format for Subchannel-QDIO description Block;]

Delete the paragraph at page 6, lines 13-16, and replace with the following replacement paragraph:

--As can be seen in Figure 1, it is also possible to have one or more dynamic switches 160 or even a switching fabric (network of switches) included as part of the path, coupled to the channel(s) 155 and the control units(s) 180. Each control unit 180 is further attached via a bus to one or more I/O device(s) 190.--

The four replacement paragraphs at page 12, line 12 to page 14, line 26:

Figure 3 depicts the control structure overview for the input and output queues associated with a QDIO subchannel. Figure 3 also demonstrates the queue components as defined for the present invention. The Queue Information Block (QIB) [shown at 310] contains information about the collection of QDIO input and output queues associated with a given subchannel. It provides information for collection of input and output queues for the adapter associated with the subchannel. One QIB is defined per QDIO subchannel; Figure 9 provides the format of queue-information block as per one embodiment of the present invention.

The Storage List Information Block (SLIB) [shown at 320] provides for the address of information stored pertaining to each queue. One SLIB is defined for each queue. SLIB contains information about a QDIO queue and has a header and entries called storage-list-information-block entries containing information about each of the buffers for each queue. Figure 10 provides SLIB format as per one embodiment of the present

invention. Furthermore, a storage list information block element or SLIBE can be provided containing information regarding the QDIO data buffer as determined by the corresponding SL entry. Figure 11 depicts a sample SLIBE content.

The Storage List or SL [shown at 330] defines the SBAL or storage block address lists that are defined for each I/O buffers associated with each queue. One SL is defined for each queue which contains an entry for each QDIO-I/O buffer associated with the queue. SL provides information about the I/O buffer locations in main storage. As per one embodiment of the present invention, Figure 12 provides a sample SL content. SL also provides the absolute storage address of a storage block address list. In turn, SBAL contains a list of absolute addresses of the storage blocks that collectively make up one of the data buffers associated with each queue [as shown at 340]. A storage block address list entry or SBALE is also provided as part of each SBAL. Each SBALE contains the absolute storage address of a storage block. Collectively, the storage blocks addressed by all of the entries of a single SBAL constitute one of the many possible QDIO buffers of a QDIO queue. In a preferred embodiment, the number of these possible QDIO buffers equal 128. Figure 13 provides for the format of a SBALE as provided by one embodiment of the present invention. SBALF or SBAL Flags contain information about the overall buffer associated with the SBAL containing each SBALE, and not just about the storage block associated with each SBALE. The description of contents of the SBALF field is different for each SBALE within the SBAL.

A Storage-List-State Block or SLSB [is shown at 350. The SLSB] contains state indicators that provide state information about the QDIO buffers that make up a queue. A QDIO buffer consists of the collection of storage blocks that can be located

using all of the addresses in a single storage-block-address list. Depending on the current state value in an SLSB entry, either the program or the QDIO control unit can change the state of the corresponding QDIO buffer by storing a new value in the entry. Figure 14 provides a sample SLSB format as per one embodiment of the present invention. SLSB also provides for a SQBN or state of queues buffer N which provides the current state of the corresponding QDIO buffer. The QDIO buffer that corresponds to a given SLSB entry is determined by the storage list entry having the same sequential position in the storage list as the SQBN field has in the SLSB. In one embodiment, the state value consists of two parts, bits 0-2 indicate whether the buffer is owned by the program or the QDIO control unit and whether the buffer is an input or output buffer. Bits 3-7 contain a value that indicates the current processing state of the buffer. In this embodiment different bits can also be identified to mean different configurations. For example, bit zero can be established to indicates program ownership, while bits 1 and 2 provide for QDIO control unit ownership and buffer type respectively. Bits 3-7 can contain a binary value that indicates the current processing state of the associated buffer such as empty (available for data storage), primed (available to be processed), not initialized (not available for use), or halted (contains valid data but data transfer was prematurely halted by program executing Halt Subchannel), and Error (associated buffer is in an error state and contents of buffer are not meaningful).

The two replacement paragraphs at page 27, lines 13 to page 28, line 3:

The CHSC command is used to obtain self description information for the QDIO adapters associated with a specified

range of subchannels. When the CPC is operating in a mode where several images are used, the CHSC command is used to obtain self description information for the QDIO adapters associated with a specified range of subchannel images, configured to the logical partition that executed the command information for subchannel images configured to other logical partitions, if any, is not provided. Figure 5[A] represents the format for the command request block for store-subchannel-QDIO data. Figure [5B] 6 represents the format for the command response block for the store-subchannel-QDIO data command. In addition, Figure 6 [represents the format for] includes Subchannel-QDIO description Block.

In short the CHSC command specifies which device the request for processing can be sent to. It further provides for the format and attributes of the QDIO, such as the size and attribute of the queues, and other characteristics that may relate to the specific processor. QFMT or QDIO Queues Format and QDIOAC or QDIO Adapter characteristics in the [above figures represent] Subchannel-QDIO description Block of Figure 6 includes this information. IQCNT of the Subchannel-QDIO description Block provides the Input Queues Count and OQCNT also of the Subchannel-QDIO description Block provides an Output Queue Count.

VERSION WITH MARKINGS TO SHOW CHANGES MADE TO THE CLAIMS

1. (Amended) In a network computing system, an apparatus for providing direct processing access between [a] application servers and application users comprising:

a main storage capable of establishing processing communication with [an] more than one application server;

said main storage containing a queuing mechanism for retrieval and storage of incoming and outgoing data without causing interrupts in any running programs;

an interface element capable of establishing processing communication [with] between said queuing mechanism and at least one application user;

an interrogator operating independent of any application server for examining multiple queues in said queue mechanism to transfer appropriate requests, responses and data between said application [server(s)] servers and said application user(s).

2. (Amended) The apparatus of claim 1, wherein said Interface Element further comprises [of] a Connector Interface Element and a Network Interface Element.

3. The apparatus of claim 2, wherein said Connector Interface Element is in processing communication with said main storage via a Self-Timed Interface or an STI bus.

4. The apparatus of claim 2, wherein said Connector Interface Element comprises a plurality of processors.

5. The apparatus of claim 4, wherein one of said plurality of processors is used for redundancy purposes.

6. The apparatus of claim 2, wherein said main storage can be in processing communication with a plurality of network elements and servers.

7. (Amended) The apparatus of claim 6, wherein said plurality of [networks] network elements comprise at least a [web-servers] web-server.

8. The apparatus of claim 7, wherein said web-server is a TCP/IP oriented server.

9. (Amended) The apparatus of claim 2, wherein said Connector Interface Element and said Network Interface [Elements] Element are in processing communication with one another via a Peripheral Controller Interface bus or a PCI bus.

10. (Amended) The apparatus of claim 2, wherein said Network Interface Element further comprises an I/O device [adapters] adapter, at least one more processor and a local storage area.

11. The apparatus of claim 10, wherein said Network Interface Element is capable of connecting to one or more individual application users.

12. (Amended) The apparatus of claim 1, wherein said Interface Element performs [only a few special] computing network environment functions establishing network communications between said application server(s) and said application user(s) [that replace multitudes of channel functions normally performed by said computing network environment].

13. (Amended) The apparatus of claim 1, wherein said Interface Element performs [special] control unit functions [that replace many functions normally performed by one or more control units].

14. (Amended) In a network computing system having a main storage capable of connecting to [at least] more than one application server and an interface element with at least one adapter capable of establishing processing communication with at least one application user(s), an apparatus for providing direct processing access between said main storage and said adapter comprising:

data receivers set up in each of said application servers for processing data;

a plurality of queues located in main storage for providing continuous running of programs without interruptions;

an updator for changing the status of said network computing system every time new data is received, deleted or modified;

an interrogator operating independent of any application server for interrogating multiple existing queues in said main storage simultaneously to process any received data or requests such that data or requests may be received from more than one application server;

a determinator for interrogation and routing of data to appropriate application user to which said data has [to be] been forwarded [to].

15. (Amended) The apparatus of claim 14, wherein said Interface Element further comprises [of] a Connector Interface Element and a Network Interface Element.

16. The apparatus of claim 15, wherein said Connector Interface Element is in processing communication with said main storage via a Self-Timed Interface or an STI bus.

17. The apparatus of claim 15, wherein said main storage can be in processing communication with a plurality of network elements and servers.

18. (Amended) The apparatus of claim 15, wherein said Connector Interface Element and said Network Interface [Elements] Element are in processing communication with one another via a Peripheral Controller Interface bus or a PCI bus.

19. (Amended) The apparatus of claim 15, wherein said Network Interface Element further comprises an I/O device [adapters] adapter, at least one more processor and a local storage area.

20. The apparatus of claim 19, wherein said Network Interface Element is capable of connecting to one or more individual application users.

21. The apparatus of claim 15, wherein said Connector Interface Element is in processing communication with said main storage via a direct access memory I/O device.

22. (Amended) The apparatus of claim 15, wherein said Connector Interface Element and said Network Interface [Elements] Element are in processing communication with one another via a direct access memory I/O device.